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On the Baliga's Figure-Of-Merits (BFOM) Enhancement of a Novel GaN Nano-Pillar Vertical Field Effect Transistor (FET) with 2DEG Channel and Patterned Substrate

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Abstract

A novel enhancement-mode vertical GaN field effect transistor (FET) with 2DEG for reducing the on-state resistance (R_{ON}) and substrate pattern (SP) for enhancing the breakdown voltage (BV) is proposed in this work. By deliberately designing the width and height of the SP, the high concentrated electric field (E-field) under p-GaN cap could be separated without dramatically impacting the R_{ON} , turning out an enhanced Baliga's Figure-Of-Merits (BFOM, BV^2/R_{ON}). Verified by experimentally calibrated ATLAS simulation, the proposed device with a 700-nm-long and 4.6- μ m-width SP features six times higher BFOM in comparison to the FET without patterned substrate. Furthermore, the proposed pillar device and the SP inside just occupy a nano-scale area, enabling a high-density integration of such devices, which renders its high potential in future power applications.

Keywords: GaN, FET, Nano-pillar, Patterned substrate

Background

Nowadays, wide bandgap semiconductors such as ZnO, In_2O_3 , SiC, and gallium nitride (GaN) have attracted attention [1–5]. Whereas, considering the electronic properties, the lateral AlGaN/GaN high electron mobility transistor (HEMT) is widely considered as a potential candidate for substituting the Si-based device in power or frequency applications due to the higher breakdown voltage (BV) as well as the stronger thermal stability. A lot of efforts, such as p-type cap [6, 7], fluorine ion implantation [8, 9], thin barrier [10, 11], double channel [5, 12], and field-coupled gate [13], have been made on the realization of the enhancement-type HEMT that is desired to simplify the driver circuit.

These technologies face, however, many formidable challenges such as low uniformity of the threshold voltage, the waste of vertical chip area, current collapse, limited Baliga's Figure-Of-Merits (BFOM), and so on.

Especially, the contradiction between the drift length and the BV negatively influences the scaling-down of the device [14, 15]. In other words, smaller device leads to lower BV, in which it is harder to adopt the junction terminals that promote the BFOM by optimizing the electric field distribution. To this end, back barrier [16], buried junction [17], quantum well field plate [18], and other structures that are inserted into the lateral HEMT exhibiting the feature of the electrical field plate have been proposed to enhance BV by utilizing the vertical region of the chip.

On the other hand, by the virtue of the superior natures of GaN, the bulk GaN vertical field effect transistor (VFET) attracts more and more attention due to the easier realization of enhancement-type functionality and the full utilization of the vertical region [19–22]. Many novel structures are presented by experiments or simulations to incline the BV and simultaneously reduce the on-state resistance (R_{ON}) [23–25]. However, not to mention the difficulties in fabricating the super-junction (SJ) in GaN, the lack of the high-mobility two-dimensional electron gas (2DEG) leads to a higher R_{ON} [26], which hinders the optimization of BFOM in such devices.

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In this work, a novel enhancement-mode vertical GaN FET with 2DEG for reducing the R_{ON} and substrate pattern (SP) for enhancing the BV is proposed, wherein the combination of the 2DEG channel and the SP effectively balances the contradiction between the low on-state resistance and the high BV. Furthermore, the proposed device pillar and the SP inside just occupy a nano-scale area, enabling a high-density integration of such devices. Verified by numerical simulation constructed in ATLAS, the proposed device features higher BFOM compared with the same field effect transistor (FET) without the patterned substrate, rendering its high potential in future power applications.

Method

The proposed device is generated in a normal $\text{Al}_{0.23}\text{GaN}$ /GaN wafer with a highly concentrated n-type substrate acting as the drain electrode as shown in Fig. 1a, where the thickness of the layer silicon nitride (SiN), AlGaN, and GaN are 105 nm, 20 nm, and 5 μm , respectively. A n-type GaN with $2 \times 10^{16} \text{ cm}^{-3}$ doping n_D and a p-type GaN cap with $2 \times 10^{17} \text{ cm}^{-3}$ doping n_A is set as the buffer and the composite channel respectively [27, 28]. Another component of the channel beside the gate is a thin AlGaN layer which is introduced for inducing 2DEG as shown in Fig. 1b. A SP, made by aluminum oxide (Al_2O_3) for example in this paper, is grown on the substrate.

The whole device therefore could be fabricated by a standard process successively: (1) the epitaxial deposition of the conduction substrate and the integrate SP layer, (2) the partial etching of the SP pattern, (3) the deposition and polishing of n-GaN buffer, (4) the deposition of AlGaN barrier and p-GaN cap, and (5) the fabrication of electrodes and passivation.

The implanted ATLAS simulator is calibrated by the experimental data from an enhancement-type HEMT

with a p-GaN cap [29, 30]. The calibrated and other specifications of the device are shown in Table 1. Other configurations could be found in our previous work [31]. Type and density of the interface trap located at the SP/GaN interface are referred to capacitance-based experimental measurements [32–34]. The polarization charge on the AlGaN/GaN surface is confirmed according to the corresponding simple quadratic fitting equation [35].

Physics Mechanism

In on-state, compared with the device without the 2-DEG channel and the SP, the proposed vertical field effect transistor with substrate pattern (SP-VFET) features a highly conductive path owing to the 2-DEG and a narrower vertical current channel that shrinks the conductance as shown in Fig. 2. In detail, thanks to the high-density 2DEG concentrated at the AlGaN/GaN interface, the lateral path of the current flow could be sustained, which partially compensates the whole device conductance. In contrast, the current transportation capability of the SP-VFET device without 2DEG channel would be influenced dramatically.

The length of the p-GaN cap would not dramatically influence the concentration of electric field (E-field) until the length is longer than 700 nm by which the p-GaN almost covers the whole device surface. As shown in Fig. 3, the E-field distribution along the AlGaN/GaN interface owns a peak around the right corner of the p-GaN. The position of the peak shifts along with the varying p-GaN length, and however, keeps the same magnitude. Tiny difference of the peak value could be seen in Fig. 3 when the p-GaN cap is longer than 600 nm, because the long p-GaN cap flattens the whole E-field in the device and hereby expands the resistance of the device due to the depletion of the 2DEG.

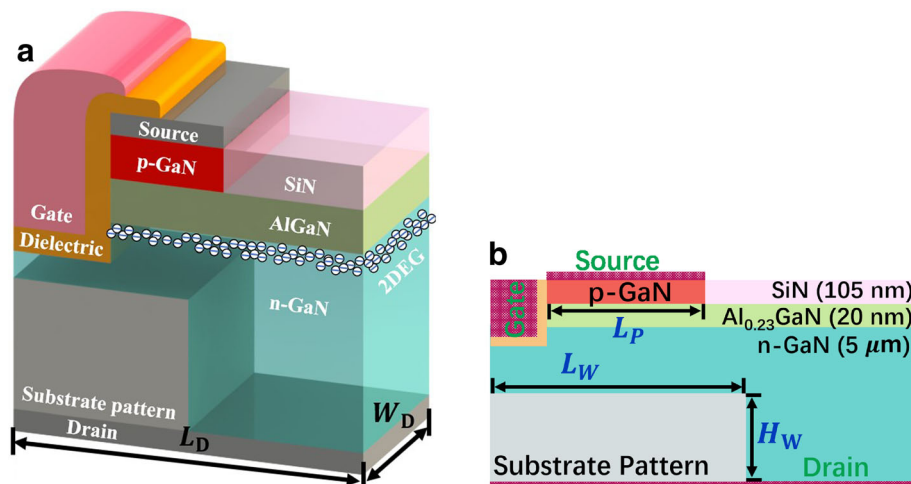
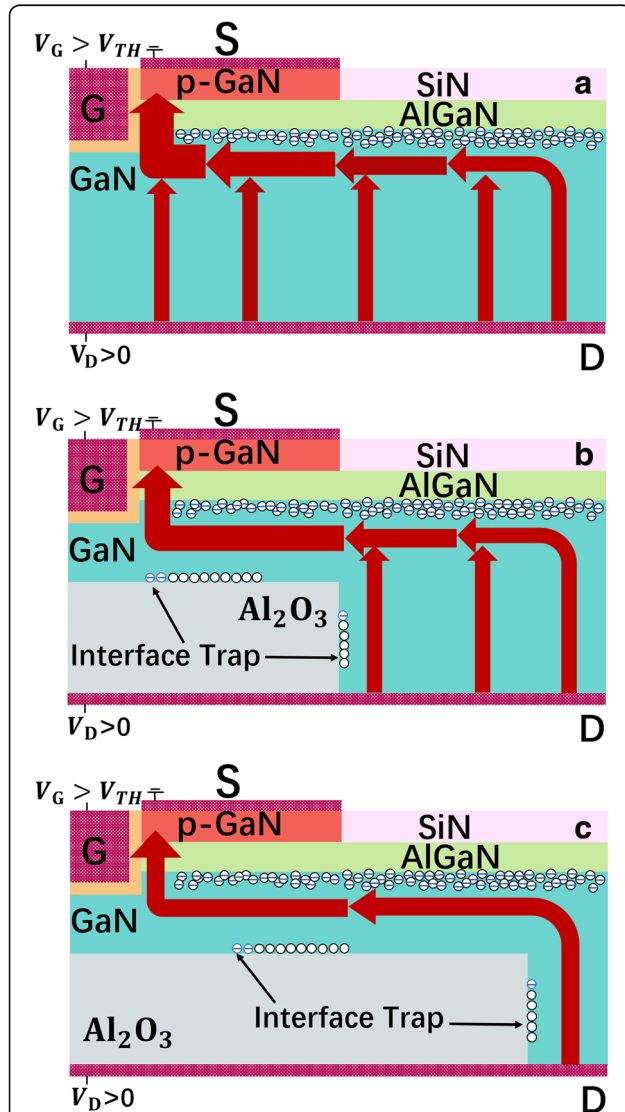
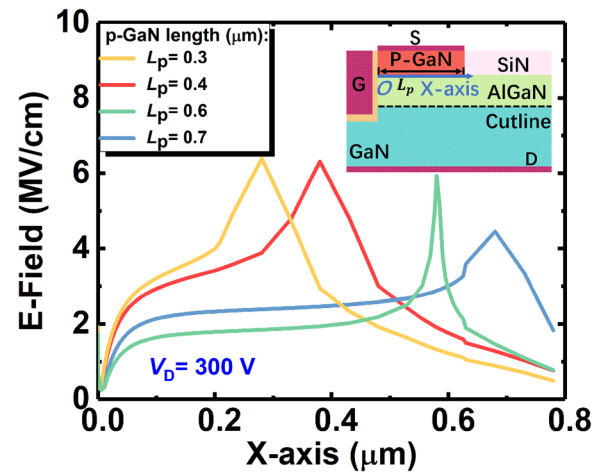


Fig. 1 The schematic **a** 3D pillar structure and **b** cross-section with labeled geometric parameters of the proposed SP-VFET

Table 1 Device specifications

Parameter	Value and unit
Device length	$L_D = 1 \mu\text{m}$
Device depth	$W_D = 1 \mu\text{m}$
Polarization charge	$\sigma_p = 6.5 \times 10^{12} \text{ cm}^{-2}$
SP interface trap (Al_2O_3)	$D_{\text{SP}} = 8 \times 10^{12} \text{ cm}^{-2}$; $E_T = E_C - 0.5 \text{ eV}$
p-GaN cap length	$L_p = 0.4 \text{ to } 0.7 \mu\text{m}$
SP length	$L_W = 0 \text{ to } 800 \text{ nm}$
SP height	$H_W = 0 \text{ to } 4.7 \mu\text{m}$
Gate length	$L_G = 15 \text{ nm}$
Gate height	$L_W = 0.17 \mu\text{m}$

**Fig. 2** The schematic illustration of the forward current flow in **a** the device without the SP, **b** the proposed SP-VFET with a short SP, and **c** a long SP**Fig. 3** The electric field distribution of the device without the SP along the AlGaIn/GaN heterojunction in different p-GaN length

To illustrate the influence of the simultaneously introduced p-GaN, 2-DEG, and the SP, an on-state conduction model can be built, as schematically shown in Fig. 4a. M_1 and M_2 are the MIS-like transistors with the conduct-channel formed in p-GaN and AlGaIn respectively. R_1 represents the infinitesimal part of vertical resistance in bulk GaN. R_2 and R_3 represent the infinitesimal resistance parts of 2-DEG channel with and without being partly depleted respectively. According to the law of resistance, R_1 , R_2 , and R_3 can be obtained as

$$R_1 = \frac{1}{n_1 q \mu} \cdot \frac{l}{dx \cdot W_D}$$

$$R_2 = \frac{1}{n_2 q \mu} \cdot \frac{dx}{t \cdot W_D}$$

$$R_3 = \frac{1}{n_3 q \mu} \cdot \frac{dx}{t \cdot W_D}$$

where n_1 , n_2 , and n_3 represent the electric concentration in GaN, undepleted 2-DEG, and depleted 2-DEG respectively; q is the electron charge and μ is the mobility of electron in GaN; l is the length of vertical conductive path and dx is the infinitesimal length in horizon; W_D is the width of the device; and t is the thickness of the 2-DEG. For convenience, t is set to be 10 nm [7]. The concentration of the depleted 2-DEG under p-GaN n_3 equals the undepleted concentration n_2 minus the total negative charge in the depleted p-GaN [31], which reads

$$n_3 = n_2 - n_A x_D$$

The p-GaN cap can be regarded as fully depleted, thus x_D equals 105 nm, the thickness of p-GaN. Compared with R_1 , R_2 and R_3 are much lower than R_1 , because of

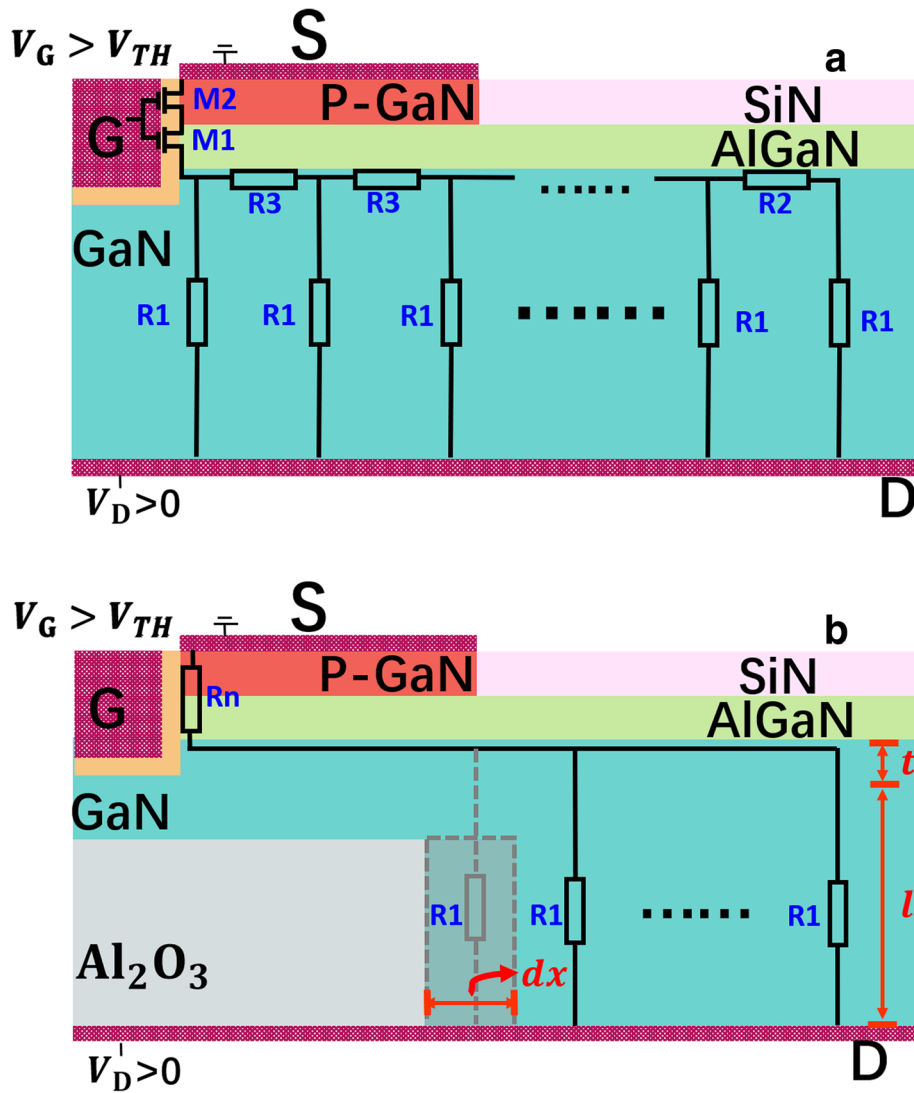


Fig. 4 The schematic of **a** proposed on-state model without SP **b** on-state resistance network model with SP

their higher electron concentration and shorter conductive path. Therefore, the resistance in the 2-DEG channel can be ignored. In addition, when the drain voltage is small and the MIS-like transistors M_1 and M_2 work in the unsaturated model, the on-state resistance of M_1 and M_2 can be regarded as an ignorable constant resistance R_n . To simplify the calculation, the analytical form of vertical current path conductance G_v of vertical current path can be obtained as

$$G_v = \int_0^{L_D} \frac{1}{R_1} = \int_0^{L_D} n_1 q \mu \cdot \frac{dx \cdot W_D}{l}$$

where L_D is the length of the device.

Therefore, the on-state resistance R_{on} can be obtained, which reads

$$R_{on} = \frac{1}{G_v} + R_n = \frac{1}{n_1 q \mu} \cdot \frac{l}{L_D \cdot W_D} + R_n$$

When SP exists, as shown in Fig. 4b, the vertical conductive path has been blocked partially. Thus, the conductance of vertical current path can be expressed as

$$G_v = \int_{L_W}^{L_D} \frac{1}{R_1} = \int_{L_W}^{L_D} n_1 q \mu \cdot \frac{dx \cdot W_D}{l}$$

where L_W is the length of the SP.

Therefore, the corresponding R_{on} can be expressed as

$$R_{on} = \frac{1}{G_v} + R_n = \frac{1}{n_1 q \mu} \cdot \frac{l}{(L_D - L_W) \cdot W_D} + R_n$$

In off-state, due to the capacitor-like functionality and the negatively charged interface trap, the SP would

redistribute the electric field under the p-GaN cap effectively, turning out a field concentration around the SP that owns wider band gap as shown in Fig. 5. Such E-field redistribution shrinks the depletion region that appears around p-GaN and the gate, and thereby relieves the high field concentration around the p-GaN cap and the gate, which would enhance the BV of the SP-VFET remarkably. On the other hand, as mentioned above, the SP would influence the device conductance such that the negative charge introduced by the SP leads to the increase of potential energy near the gate, which accounts for the decrease of 2-DEG near the gate. As a result, a

fluctuant BFOM would be achieved with varying the length and the height of the SP.

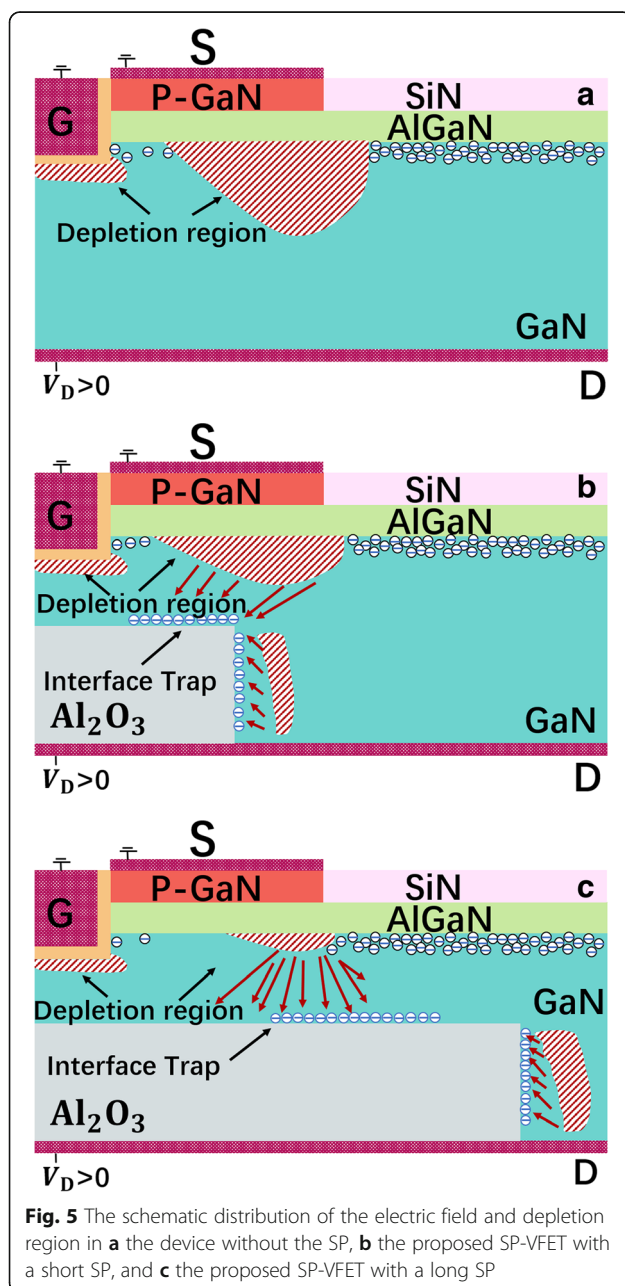
In other words, the SP could reduce the peak of the E-field around the p-GaN corner and simultaneously, attract the E-field concentrating across the SP, as shown in Fig. 6a, b. However, thanks to the higher critical E-field of the SP, such E-field concentration would not break the device, by which the SP-VFET would exhibit much higher BV.

Result and Discussion

Figure 7a, b respectively shows the transfer and output curves of the proposed device without the SP. With different length of the p-GaN cap, these curves overlay each other in both subthreshold and turn-on regimes, suggesting the length of the p-GaN cap does not influence the conductance of the device without the SP. In other words, although the p-GaN cap would partially deplete the 2-DEG and hereby affect the resistance of the 2-DEG channel, the remained 2-DEG still owns a large concentration n_3 that approximates the undepleted concentration n_2 , which is realized by optimizing the p-type concentration in p-GaN cap. Furthermore, as analyzed before, the resistance of the 2-DEG channel is rather small compared with the resistance of the n-GaN in vertical path. Therefore, the transfer curves overlay each other in Fig. 7a, b. However, in order to protect the gate from the highly concentrated E-field, such crowding should not be adjacent to the gate, which means the length of the p-GaN could not be too short. Thus, the minimum length of the p-GaN in our work is 400 nm unless otherwise stated.

Figure 8 shows the output characteristics of the proposed SP-VFET and the VFET without the SP. It can be seen that the SP does impose the device resistance by narrowing the vertical conduction channel. In detail, the on-state resistance is independent to the height of the SP when the height is below 4.7 μm , while, significantly depends on the length of the SP which matches the mechanism that narrow vertical current path shrinks the conductance. The former independency is because the 2DEG is the main lateral conduction channel that would not be weakened by the SP within its moderate height. However, if the SP is adjacent to 2-DEG channel, the introduced negative charge around the SP will level up the energy band, resulting in the dramatical decrease of the 2-DEG concentration. Consequently, the resistance of the 2-DEG increases and the total on-state resistance R_{on} increases accordingly. Besides, the later dependency comes from the remarkably boosted resistance in the vertical channel as aforementioned. Furthermore, it should be noted that the lattice defects in 2-DEG induced by high SP limit the height of SP.

Figure 9 shows the details of the current density distribution around the gate of the VFET devices with or



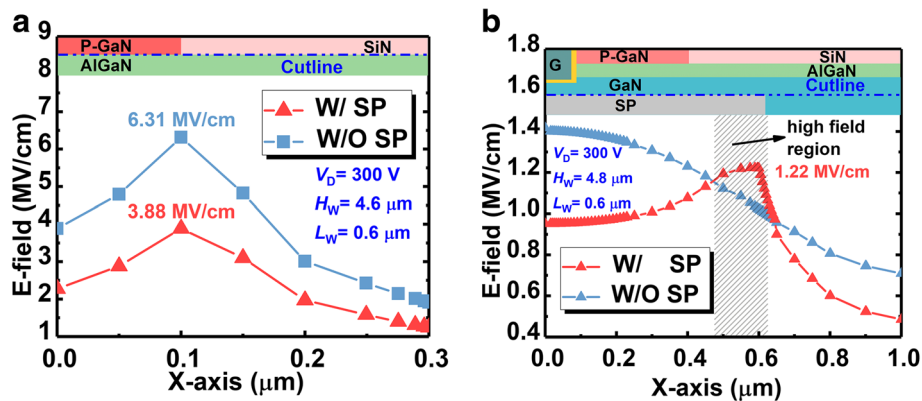


Fig. 6 The electric field distribution of the proposed SP-VFET along the interface of **a** p-GaN/AlGaIn and **b** GaN/SP

without the SP, wherein the VFET without the SP has a higher current transportation capability which keeps in line with Fig. 8a. And oppositely, the SP-VFET shrinks the current conduction by narrowing the vertical channel. Meanwhile, the detailed figures clearly illustrate that the current in the lateral channel is transported by the

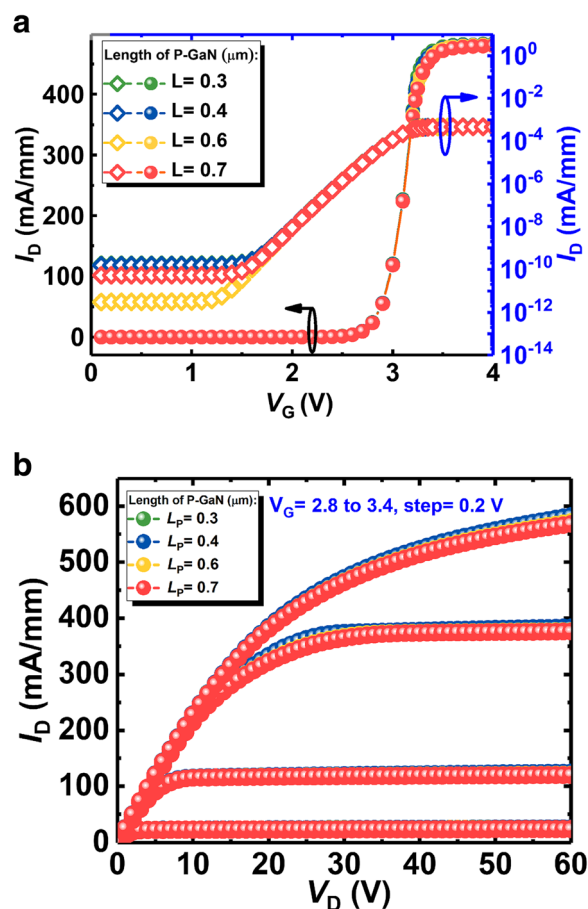


Fig. 7 **a** The transfer curves and **b** output curves of the device without the SP in different length of the p-GaN cap

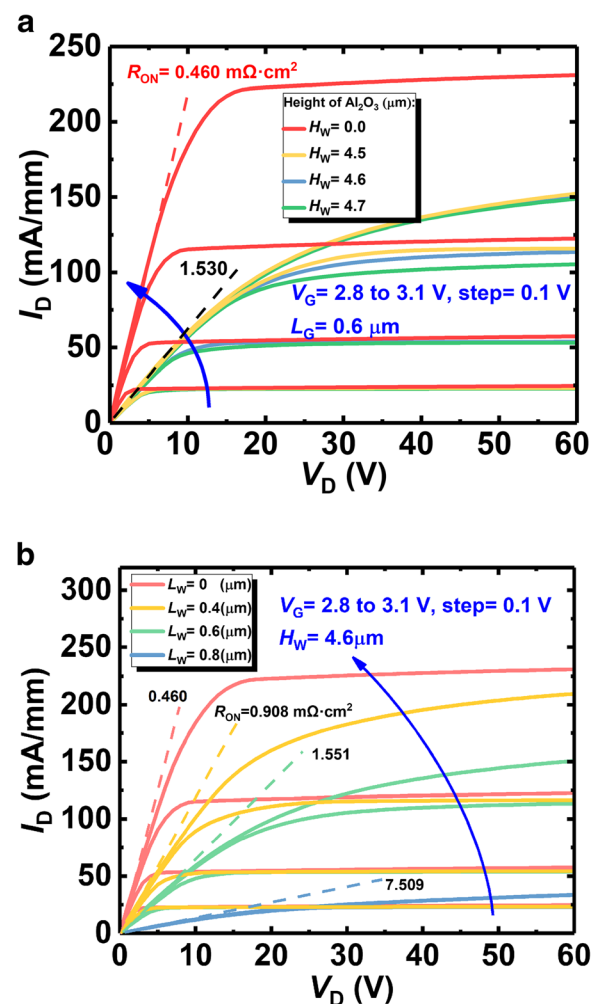
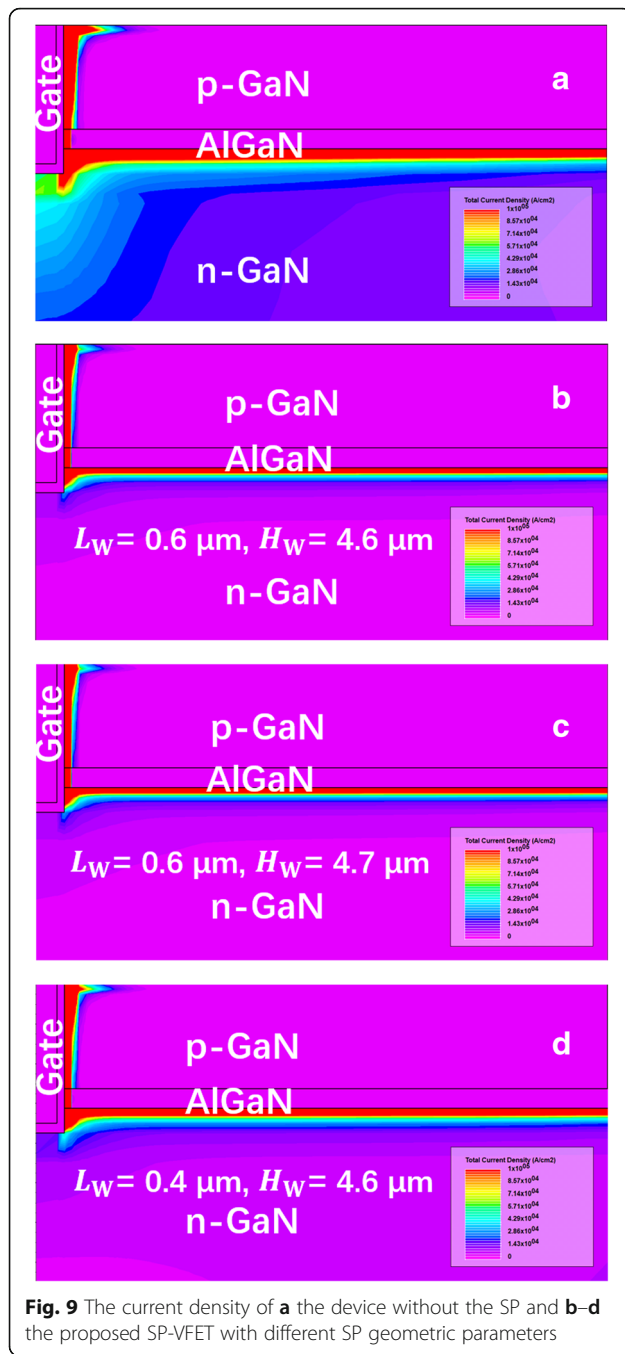
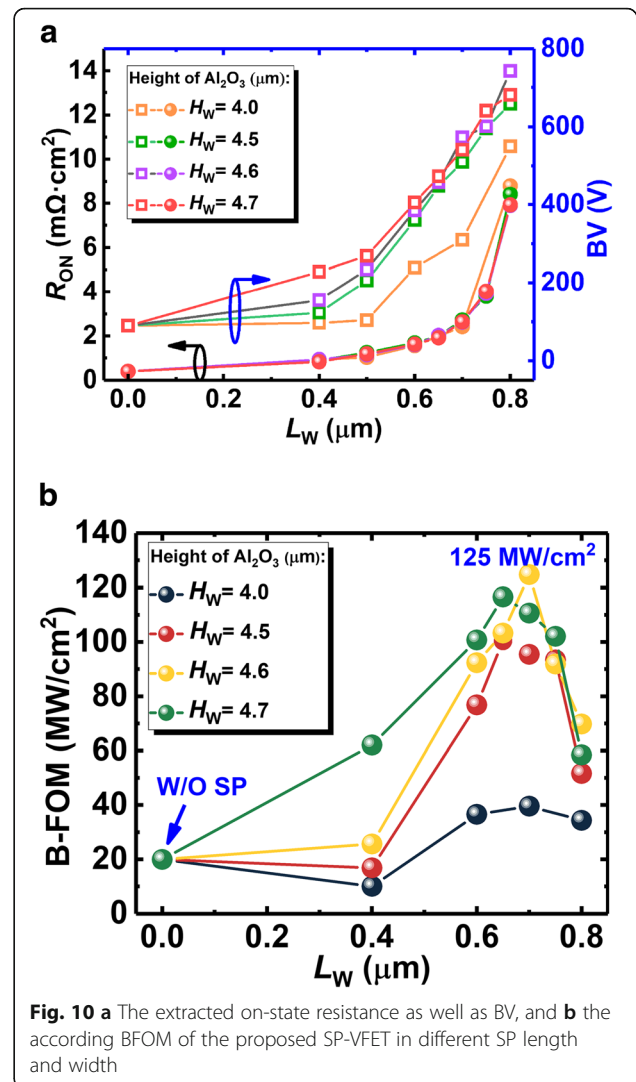


Fig. 8 The output curves of the proposed SP-VFET with varying **a** SP width and **b** SP length compared with the device without SP



2DEG, and the total current density changes slightly with growing SP height, which is also demonstrated in the mechanism section. The results indicate the lateral channel resistance is not imposed notably by the SP within moderate height.

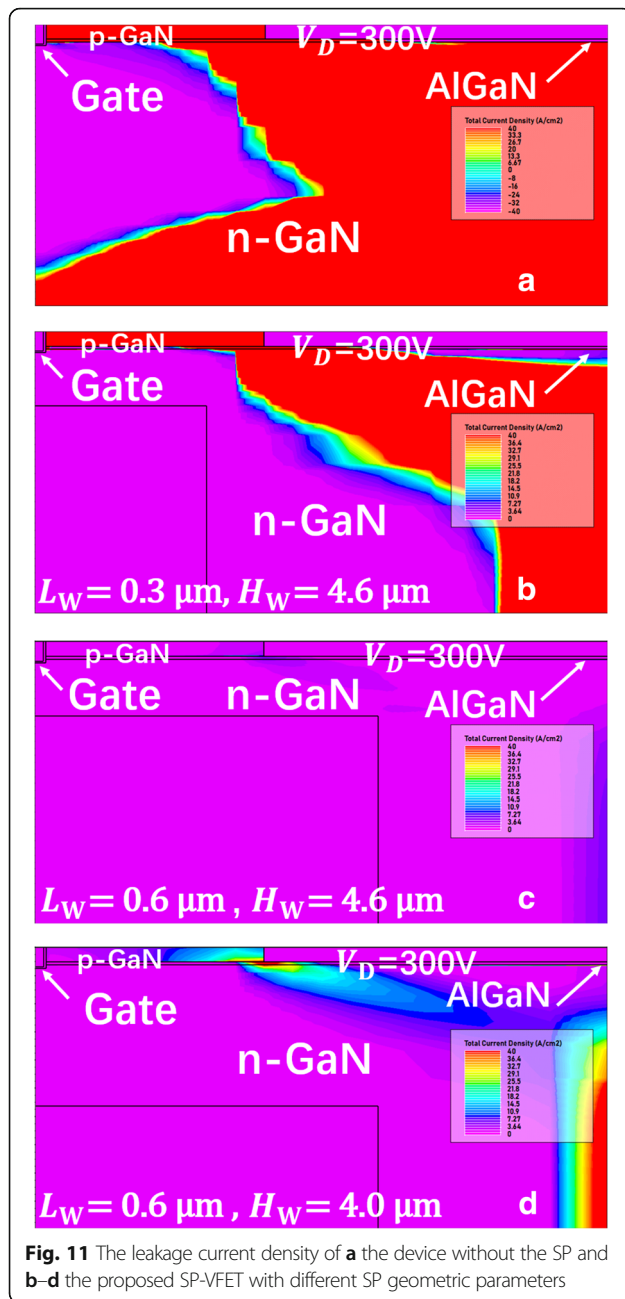
Figure 10a shows the extracted on-state resistance and the corresponding BV. The resistance of the SP-VFET increases with longer SP. And especially, the curve of the resistance versus SP length exhibits a hyperbolic trend, and the gradient of the curve increases with the longer SP



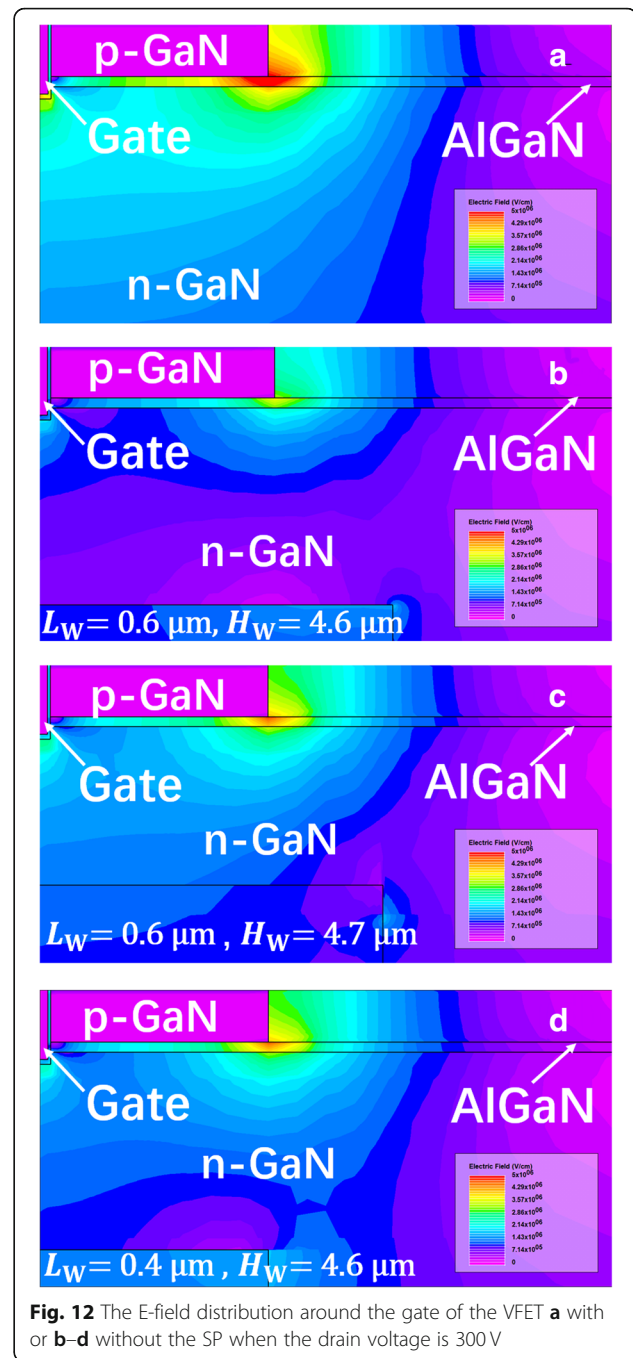
length. As analyzed before, R_{on} varies with different SP length L_W in a form of hyperbolic function, which matches the simulation result. Moreover, the curve of the resistance with different SP heights overlays each other as the height is lower than 4.7 μm , suggesting that 2-DEG channel is the main lateral conductive path and the 2-DEG channel is not affected, as mentioned above.

Figure 10b shows the calculated BFOM of the SP-VFET. Owing to the different increasing rate of BV and on-state resistance, the BFOM of all the devices firstly grow and then drop after the length of the SP longer than 400 nm. A peak BFOM of 125 MW/cm^2 is achieved when the length reaches 700 nm and the height reaches 4.6 μm . Compared with the device without the SP, the proposed SP-VFET performs more than six times better in terms of the BFOM.

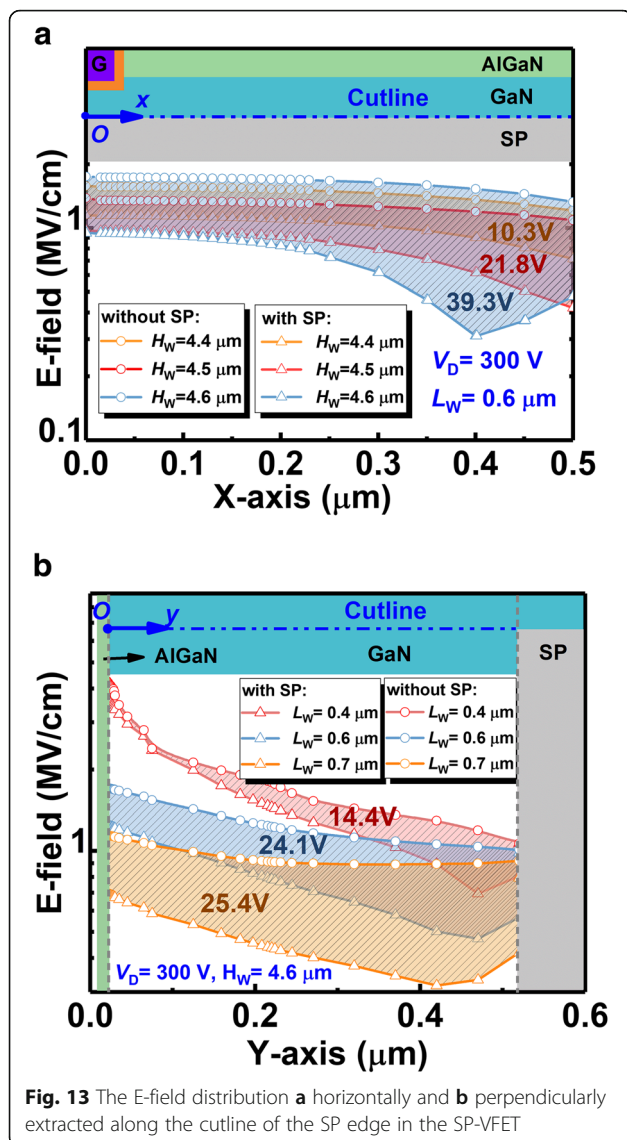
This improvement is achieved owing to the suppression of the high E-field under the p-GaN, thanks to the negatively charged interface trap around the SP. The



interaction, which occurs between the trapped negative charge on the interface of the SP and the depletion region around the p-GaN, forms a new distribution of E-field mainly towards the trapped charge. According to the Gauss' law, the electric flux is limited by the charge encircled. Thus, the introduced E-field will affect the electric flux toward elsewhere. As the negative charge of depletion region is the main source for the crowded E-field around p-GaN, the E-field introduced by the trapped charge will play a role in suppressing the E-field crowded around p-GaN, and consequently, BV is enhanced. Specifically, when the SP length is lower than



400 nm, the negative charge introduced by SP is far away from the depletion region. Thus, the E-field formed between the depletion region and trapped negative charge is too small to play a role in affecting the crowded E-field under p-GaN. And as a result, the BV of the device grows slightly. However, as the SP length is higher than 400 nm, owing to the more trapped negative charge on the interface of the SP and shorter distance between the depletion region and trapped negative charge, the



E-field between the depletion region and trapped negative charge is enhanced, leading to the growth of the BV.

Additionally, the region around the SP is tremendously depleted due to the negative charge introduced by SP. And as shown in Fig. 11, with the longer SP, the vertical leakage current path constricts in width owing to the depleted region squeezing to the device edge, which also block the leakage current, and consequently enhance the BV. Therefore, the BV rises remarkably with the increasing SP length.

Figure 12 shows the simulated E-field distribution in the SP-VFET when the drain voltage is 300 V, where apparently the SP induces other new E-field concentration points, meaning that the peak E-field region under the p-GaN is suppressed. Compared with the E-field distribution in the devices with different SP height, the increase of SP length suppresses the congregation of E-field and consequently enhances the BV more efficiently.

Such flattened E-field could also be observed explicitly in Fig. 13, in which the E-field distributions along the horizontal and perpendicular edge of the SP (see the cutline) are plotted. As demonstrated in polychrome Fig. 12, it can be seen in Fig. 13 that higher and longer SP plays a more and more effective role in reconstructing the E-field under p-GaN, and, attracting E-field to concentrate across the SP edge. This redistribution counteracts the E-field around vulnerable p-GaN. Thus, the BV of the device is enhanced, boosting the B-FOM of proposed SP-VFET.

Conclusion

In this work, a novel enhancement-type GaN vertical FET (SP-VFET) with 2DEG channel and substrate pattern for improving the BFOM thereof is proposed and investigated. Verified by experimentally calibrated simulation implemented with ATLAS, it is the SP that relieves the E-field peak under the p-GaN, and simultaneously, attracts new E-field concentration across the SP that owns higher critical E-field. Consequently, the BV of the proposed SP-VFET is boosted with a moderately increasing on-state resistance due to the 2DEG compensation. The BFOM of the SP-VFET therefore is enhanced six times better than that of the device without the SP when the SP length and height are 700 nm and 4.6 μm respectively, rendering the promising potential of the proposed SP-VFET in high-density power integration.

Abbreviations

n_A : Doping concentration of p-type GaN; n_D : Doping concentration of n-type GaN; 2DEG: Two-dimensional electron gas; $\text{Al}_{0.23}\text{Ga}_{0.77}\text{N}$: Aluminum gallium nitride with a mole fraction of 0.23 for aluminum; Al_2O_3 : Aluminum oxide; BFOM: Baliga's Figure-Of-Merits; D_{ST} : Interface trap density of the substrate pattern; E-field: Electric field; E_f : The difference between the conduction band and interface-trap energy-level; FET: Field effect transistor; GaN: Gallium nitride; HEMT: High electron mobility transistor; H_G : Height of the gate; H_W : Height of substrate pattern; L_D : Length of the device; L_G : Length of the Gate; L_P : Length of the p-GaN cap; L_W : Length of the substrate pattern; SiN: Silicon nitride; SP: Substrate pattern; SP-VFET: Vertical field effect transistor with substrate pattern; W_D : Depth of the device; σ_p : Polarization charge

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Availability of Data and Materials

The data generated during and/or analyzed during the current study are available from the corresponding authors on reasonable request.

Authors' Contributions

ZW brought out the idea of the structure and supervised the simulation. ZW and ZZ carried out the simulations and analysis. DY created the figures and wrote the manuscript. YY supervised the whole work. All authors discussed the results and contributed to the final manuscript. All the authors have read and approved the final manuscript.

Competing Interests

The authors declare that they have no competing interests.

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